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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,166	01/21/2004	Hsiang-Tai Lu	TS02-716	3768

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EXAMINER	
OWENS, DOUGLAS W	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/762,166	LU ET AL.	
	Examiner	Art Unit	
	Douglas W. Owens	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37 and 40-48* is/are rejected.

7)☒ Claim(s) *38 and 39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

2. The abstract of the disclosure is objected to because the first line of the abstract draws reference to purported merits of the invention. Correction is required. See MPEP § 608.01(b).

Claim Objections

3. Claims 19 – 34 are objected to because of the following informalities: In line 1 of each of the claims, "structure" should be replaced with --method--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1 – 3, 6 – 20, 23 – 37 and 40 – 48 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 18 and 35 draw reference to "type one" and "type two" isolation regions. The scope of the claims are vague, since it is not known what is meant by "type one" or "type two" isolation regions.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

7. Claims 1 – 14 and 18 – 27 are rejected under 35 U.S.C. 102(a) as being anticipated by admitted prior art, henceforth referred to as APA.

Regarding claims 1 – 5, APA teaches a structure comprising:

a silicon semiconductor region in a silicon substrate;

STI regions (4, 52) separating cells and programming bit line channel regions of a cell from reading bit line channel regions of a cell, delineating active regions contained within the semiconductor region;

a conductive floating gate (8), for each cell, having a first floating gate portion disposed over the active region in the programming bit line channel region of a cell and a second floating gate portion disposed over the active region in the reading bit line channel region of the cell, both said first and second floating gate portions being separated from the active regions by a floating gate insulator layer disposed over the active regions, and a third floating gate portion passing over the STI region to connect the first floating gate portion and second floating gate portion;

a conductive control gate (12) separated from the floating gate by an integrate insulator layer and from said semiconductor region by a control gate insulator layer and having a first control gate portion entirely disposed over the first floating gate portion, where said first floating gate portion completely covers the space between a first source region and a first drain region, having a second control gate portion disposed over said second floating gate portion, where said second floating gate portion does not extend all the way from a second source region to second drain region, said second control gate region completing the covering of the space between the second source region and the second drain region and having a third control gate portion disposed over the third floating gate portion and connecting the first control gate portion and second control gate portion;

a covering insulator layer (16) with a programming bit channel contact line (18) disposed over the covering insulator layer and connecting to the first drain region and covering insulator and a reading bit line channel contact line disposed over said

covering insulator and connecting to the second drain region through the covering insulator layer.

Since there is nothing in the claims with respect the exact boundaries of each gate portion, the portions can be nearly arbitrarily selected and meet the claim limitations.

Regarding claim 6, APA teaches a structure, wherein the floating gate is polysilicon (page 2, lines 16 and 17).

Regarding claim 7, APA teaches a structure, wherein the floating gate insulator layer is an oxide (page 2, lines 14 – 16).

Regarding claim 8, APA teaches a structure, wherein the control gate is polysilicon (page 2, lines 21 – 23).

Regarding claim 9, APA teaches a structure, wherein the control gate insulator layer is an oxide (page 2, lines 14 – 16).

Regarding claim 10, APA teaches a structure, wherein the intergate insulator is an oxide grown over the floating gate (page 2, lines 20 and 21).

Regarding claims 11 – 14, APA does not teach forming the source/drain regions by ion implantation. This is considered a product by process limitation and has not been given any patentable weight. "Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a

different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Regarding claims 18 – 22, APA teaches a method of making flash memory cells comprising:

providing a silicon semiconductor region in a silicon substrate;

forming STI regions (4, 52) separating cells and programming bit line channel regions of a cell from reading bit line channel regions of a cell, delineating active regions contained within the semiconductor region;

forming a conductive floating gate (8), for each cell, having a first floating gate portion disposed over the active region in the programming bit line channel region of a cell and a second floating gate portion disposed over the active region in the reading bit line channel region of the cell, both said first and second floating gate portions being separated from the active regions by a floating gate insulator layer disposed over the active regions, and a third floating gate portion passing over the STI region to connect the first floating gate portion and second floating gate portion;

forming a conductive control gate (12) separated from the floating gate by an integrate insulator layer and from said semiconductor region by a control gate insulator layer and having a first control gate portion entirely disposed over the first floating gate portion, where said first floating gate portion completely covers the space between a first source region and a first drain region, having a second control gate portion disposed over said second floating gate portion, where said second floating gate portion does not extend all the way from a second source region to second drain region, said

second control gate region completing the covering of the space between the second source region and the second drain region and having a third control gate portion disposed over the third floating gate portion and connecting the first control gate portion and second control gate portion;

forming a covering insulator layer (16) with a programming bit channel contact line (18) disposed over the covering insulator layer and connecting to the first drain region and covering insulator and a reading bit line channel contact line disposed over said covering insulator and connecting to the second drain region through the covering insulator layer.

Regarding claim 23, APA teaches a method, wherein the floating gate is polysilicon (page 2, lines 16 and 17).

Regarding claim 24, APA teaches a method, wherein the floating gate insulator layer is an oxide (page 2, lines 14 – 16).

Regarding claim 25, APA teaches a method, wherein the control gate is polysilicon (page 2, lines 21 – 23).

Regarding claim 26, APA teaches a method, wherein the control gate insulator layer is an oxide (page 2, lines 14 – 16).

Regarding claim 27, APA teaches a structure, wherein the intergate insulator is an oxide grown over the floating gate (page 2, lines 20 and 21).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 15 – 17 and 28 – 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA.

Regarding claim 15, APA does not teach that the insulator layer is an oxide, a nitride or an oxynitride composite layer. These are known materials that are well suited for the intended use. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use known materials that are suited for the intended use, since it is desirable to use reliable materials. The selection of a known material based on its suitability for its intended use supported a *prima facie* obviousness determination in *Sinclair & Carroll Co. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945).

Regarding claims 16 and 17, APA does not teach using polysilicon for the contact lines. Polysilicon is a known material that is well suited for the intended use, as discussed above.

Regarding claims 28 – 31, APA does not teach forming the source/drain by ion implantation. Ion implantation is a known and commonly used method of forming doped regions. It would have been obvious to one having ordinary skill in the art to use a known method of forming the source/drain regions since it is desirable to use reliable process steps.

Regarding claim 32, APA does not teach that the insulator layer is an oxide, a nitride or an oxynitride composite layer. These are known materials that are well suited

for the intended use. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use known materials that are suited for the intended use, since it is desirable to use reliable materials.

Regarding claims 33 and 34, APA does not teach using polysilicon for the contact lines. Polysilicon is a known material that is well suited for the intended use, as discussed above.

10. Claims 38 and 39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W. Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Douglas W Owens
Examiner
Art Unit 2811